ventional planar metal-oxide-semiconductor field effect transistor (MOSFET) and a semiconductor device including FinFETs according to the embodiments of the present invention.

When it is assumed that a reference channel length of a planar MOSFET of a cell region is 100 nm and a fin height of a single channel FinFET or a multi-channel FinFET is 100 nm, in the FinFET according to the third embodiment (refer to FIG. **15**), effective channel length is 300 nm. In the multi-channel FinFETs according to the first, fourth, fifth, and sixth embodiments (refer to FIGS. **10**, **19**, **31**, and **41**, respectively), effective channel length is 500 nm.

When it is assumed that a reference channel length of a planar MOSFET of a peripheral circuit region is 500 nm and a fin height of a single channel FinFET or a multi-channel FinFET is 100 nm, in the multi FinFET according to the fifth embodiment (refer to FIG. **31**), effective channel length is 1300 nm. In the plurality of single channels FinFETs according to the sixth embodiment (refer to FIG. **41**), effective channel length is 900 nm.

Further, in the multi-channel FinFETs according to the first and second embodiments (refer to FIGS. **10** and **15**, respectively), effective channel length is 1500 nm.

A semiconductor device including a multi-channel FinFET and method of fabricating the same produces the following advantages. First, because three-dimensional channels are obtained by forming central trenches in active regions in the present invention, reductions in contact areas of sources and drains may be prevented. More specifically, three-dimensional channel regions can be formed without reducing the area of active regions defined when isolation regions are formed.

Second, in the present invention, active region hard masks are isotropically etched and used as channel region defining patterns. Accordingly, the entire process can be simplified by omitting a process of coating or depositing an additional material required for forming channel region defining patterns, and, thus, fabrication cost can be reduced.

Third, fins having a uniform width can be formed by changing an edge shape of an active region of a conventional FinFET without changing the conventional layout. Therefore, a current characteristic requisite for a transistor can be stably maintained.

Fourth, as compared with when an SOI substrate is used, the semiconductor device of the present invention, which may use a bulk silicon substrate, reduces fabrication cost and avoids a floating body effect, a drop in breakdown voltage between a source and a drain, and an increase in off-current.

Exemplary embodiments of the present invention have been disclosed herein and, although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate having a cell region and a peripheral circuit region, a portion of the semiconductor substrate in the cell region and in the peripheral circuit region including an isolation region defining an active region;

portions of the active region protruding above an upper surface of the isolation region to define at least two active channels, respectively;

a gate dielectric layer over the active region of the semiconductor substrate including the at least two protruding active channels;

a gate electrode over the at least two protruding active channels, the gate dielectric layer and the isolation region of the semiconductor substrate, the gate electrode at least partially filling a trench located between a given pair of the at least two protruding active channels, the trench laterally overlapping the active region; and

a source/drain region in the active region of the semiconductor substrate on either side of the gate electrode.

2. The semiconductor device as claimed in claim **1**, wherein the semiconductor substrate is selected from the group consisting of a bulk silicon wafer, a silicon-on-insulator (SOl) substrate, a silicon germanium-on-insulator (SGOI) substrate, and a silicon germanium (SiGe) wafer.

3. The semiconductor device as claimed in claim **1**, wherein the at least two active channels are parallel.

4. The semiconductor device as claimed in claim **1**, wherein each of the at least two protruding active channels has a width of about 30 nm or less.

5. The semiconductor device as claimed in claim **1**, wherein an upper surface of the active region between the at least two protruding active channels is level with the upper surface of the isolation region in the semiconductor substrate.

6. The semiconductor device as claimed in claim **1**, wherein the active region between the at least two protruding active channels is recessed so that an upper surface of the active region between the at least two protruding active channels is lower than the upper surface of the isolation region in the semiconductor substrate.

7. The semiconductor device as claimed in claim **1**, wherein an upper surface of the active region between the at least two protruding active channels is higher than the upper surface of the isolation region in the semiconductor substrate.

8. The semiconductor device as claimed in claim **1**, wherein the at least two protruding active channels are cell region active channels formed in the cell region of the semiconductor substrate.

9. The semiconductor device as claimed in claim **8**, further comprising:

a portion of the active region in the peripheral circuit region of the semiconductor substrate protruding above the upper surface of the isolation region in the peripheral circuit region of the semiconductor substrate to define a plurality of peripheral circuit region active channels.

10. The semiconductor device as claimed in claim **1**, further comprising:

a portion of the active region in the peripheral circuit region of the semiconductor substrate protruding above the upper surface of the isolation region in the peripheral circuit region of the semiconductor substrate to define a plurality of peripheral circuit region active channels.

11. The semiconductor device as claimed in claim **10**, wherein the active region under each of the plurality of peripheral circuit region active channels is separated by the isolation region.

12. The semiconductor device as claimed in claim **1**, wherein the at least two protruding active channels are peripheral circuit region active channels formed in the peripheral circuit region of the semiconductor substrate.

13. The semiconductor device as claimed in claim **12**, wherein the active region under each of the plurality of peripheral circuit region active channels is separated by the isolation region.

14. The semiconductor device as claimed in claim **12**, further comprising: